Nicholas Paul Dietz

Internet Address
nick.dietz@gmail.com
https://www.poleguy.com
https://www.poleguy.com/resume_2024.pdf

Home Address
244 S. Wesley
Oak Park, IL 60302
Land: (708) 848-3835
Mobile: (630) 460-1424

Objective

To find an electrical engineering hardware design role working on unique and challenging engineering problems through the use of digital signal processing, hardware, and software techniques.

Relevant Work Experience

Shure Incorporated, Niles, IL (Fully remote since 2020) May '10 – August '24 (Present)
https://shure.com

Staff Engineer and Senior Staff Engineer Roles

- Currently working on next-generation modem design for a soon to be released custom low-latency pro-tier digital modem, including integration of current-technology and legacy modem support, DSP real-time power and current limiting algorithms, and user interface design.
- Support of MIMO modem development including training new employees on test-equipment usage of Spectrum Analyzers and Vector Signal Generators in the context of our custom modems.
- Set-up remote control hardware development platform for our team for the Covid lock-down. This setup was a huge success as a model for shared remote hardware development by our team, and has expanded into a full lab of remotely controlled test-beds used for development and hardware regression testing for the last four years.
- Created a third generation FPGA based gigabit-serial and Ethernet telemetry capture system ('Proton Pack') for portable modems allowing analysis of detailed modem behavior in real-world customer environments (e.g. United Center, Grand Ole Oprey, Wheaton Bible Church, Thalia Hall, Millennium Park, Drury Lane Theater, etc.).
- Created real-time live visualization system for telemetry data during walk-testing using Python, matplotlib and datashader.
- Created exploratory data analysis tools for rapid review and analysis of captured data using Python, hdf5 and datashader.
- Design, simulation and implementation of FPGA code for timing recovery, carrier recovery, equalization, encryption, diversity selection, AGC, downconversion, FEC, etc. for ULXD, QLXD, Axient Digital and other modems.
- Designed the modulation for UXLD and QLXD ISM band by expanding the standard QPSK modulation to a complex modulation.
- FPGA design and implementation for low-latency (2 msec) digital modem design measured from audio in to audio out.
- Set up the hardware lab for Shure's first 5G cellular product design for low latency (8-50 msec) audio applications. Supervised the installation of a private 5G base-station and guided system latency measurements over 3GPP 5G radios.
- Designed an implemented a second generation telemetry capture system for the Axient Digital Receiver Modem design using Dante hidden channels over Ethernet. Subsequently ported this design to support the ADX5D development. Wrote software control tools in Javascript and Node Webkit to support this platform.
- Wideband OFDMA Demonstrator: Battery system design, mechanical design, clock architecture, ZC706 based fiberoptic master with battery powered nodes. KiCad design of fiberoptic node including assembly board-bring-up and bench testing. PLL's. Asynchronous serial link design. 3D Cad design of housing using Fusion 360 and FreeCAD, and in-house CNC machining.
- Design and bring-up of custom 8-core floating-point DSP including 2MHz serial debug interface.
- Designed and implemented the algorithm for the Microbodypack tunable antenna for use on Shrek the Musical in the UK Tour in Edinburgh 2017 and subsequent public release.
- Developed state-of-the-art GAN power modules for prototypes.
- Developed KiKad based flow for same-day custom in-house laser-cut brass shield design using our LPKF Laser Material Processing machines.
- Provided design updates for AGC in support of 1.2 GHz Axient Digital Release for Tokyo Olympics.
- Traveled to MIT Media Lab to design a custom wireless glove controller sending I2S motion capture data via the ULXD modem channel to support Ariana Grande's 2015 national tour to avoid risk of using WiFi for control in stadium venues.
- Transitioned our team from a Windows based flow to a Linux centered flow for FPGA, verilog and VHDL, rtl simulation in Modelsim, xsim, GHDL, CVC, and Riviera-PRO, using Python and cocotb, and bit-exact model simulation in Python and boost C++.
- Support in selecting and hiring a tools engineer to handle our new Linux infrastructure. SGE, Slurm, Jenkins, Proxmox, Anisble, CentOS, RHEL, Ubuntu, etc.
- Created and distributed CentOS VM images as a first step to support transition to Linux based FPGA design flow.
- Set up automated regression testing hardware and developed tests to allow for nightly automated hardware tests of each FPGA build.
- Developed a framework for remote builds on a rack of Linux servers and build machines. The framework includes python

virtual environments, Xilinx Vivado and ISE tcl scripting, Jenkins and Slurm CI/CD, automated version numbering, automated deployment of FPGA images to artifactory, and automated git version control reporting.
- Traveled as needed to provide field support for NBC, Saturday Night Live, National Boxing, Australia Rules Rugby, etc.
- Supported the hiring of interns and provided internship guidance.
- Emceed the 2018 Holiday show after performing piano with various bands at several prior shows.
- Analysis of phase-step transients in temperature compensated TCXOs.
- Designed and developed a standards based 2.4GHz WiFi microphone schematic and layout.
- Designed and developed the firmware (C/ASM) for GLXD including the frequency hopping scheme, FEC, channel scan and automatic channel selection algorithms.
- Bit-serial EVM filter design.
- Shipped Shure's first UHF digital wireless microphone, ULXD.
- Developed a telemetry capture system for the ULXD platform by utilizing the Dante ethernet transport to provide real-time visualization of modem performance in the field.
- Created real-time modem telemetry visualization tool in C++ using the JUCE framework.
- Ported Matlab fft analysis code to Python and to C to create FFT analysis software for bench level debug by RF engineers.
- Created Matlab based tool for plotting and analyzing captured modem telemetry data.

Phantom Power Racing May '14 – August '24 (Present)
https://phantompowerracing.org
Founding Team Member
- Modeled, designed, simulated and built a fully-custom FPGA based three-phase motor-controller from trapezoidal and sinusoidal drive, angle sensor implementation, and PI control loop design for battery and motor current control.
- Designed and built power electronics, controls, and complete go-kart to win the national Power Wheels championship in 2014. Featured in Hot-Rod Magazine in 2014.
- Designed and built an Aluminum framed racing Ice Cream Truck with music synchronized to speed.
- 3D printed magnet mounts to drive angle sensors for alternators used as motors.

Shure Incorporated, Niles, IL April '05 – April '10
https://shure.com
Senior Engineer and Project Engineer Roles
- Worked on the design and implementation of a digital modem for a low-latency (<5ms) microphone application targeting Xilinx FPGAs, released in ULXD and later QLXD.
  Utilized Simulink and Matlab for DSP signal processing algorithm development and verification.
  Validated BER performance of 8-PSK modulation including PLL feedback-loop performance analysis, and frequency domain filter analysis.
- Designed and developed a 42-Mhz 14-bit and 16-bit ADC front end for Shure's first generation digital wireless microphone, ULXD. Was responsible for schematic design, circuit board design, board bring-up, debug and test.
- Designed and developed a real time RF fader device with hardware synchronized audio recording capability for comparative analog and digital microphone testing.
- Implemented and tested a digital modem for wireless microphone prototype using Simulink. Was responsible for providing timing closure for a complex multi-cycle Altera FPGA design using a model-based Simulink and DSPBuilder flow.
- Designed and implemented a hardware test and validation suite using Ethernet based VISA instrumentation control for logic analyzers, RF signal generators, and Matlab based data post processing.
- Designed the PCB schematic and supervised layout for Shure's first prototype digital wireless receiver hardware platform using Mentor Graphics that would later become ULXD.
- Designed the user interface panel for next-generation top tier rack mount wireless microphone receiver, Axient Digital. Was responsible for parts selection, prototyping, schematic entry, board bring-up, debug, and SPICE simulation of circuitry for IR communication.
- Developed firmware for AES-3 digital wired microphone control protocol.
- Developed FPGA code for a proprietary embedded real-time audio networking chipset.
- Developed the embedded firmware for the PG Wireless Microphone System. Implemented design using C on embedded Freescale processors.

Mindspeed Technologies, Lisle, IL July '99 – April '05
https://en.wikipedia.org/wiki/Mindspeed_Technologies
https://en.wikipedia.org/wiki/Conexant
Electrical Engineering Level I through Level III Roles.
- Led development of numerous Compact PCI cards, bench-top ASIC evaluation boards, and PCI cards. Responsibilities included schematic entry in Viewdraw and Orcad, PCB layout in PADS, board fabrication support, JTAG test development, board bring-up, PCB re-work, VHDL based FPGA design and implementation, and first-silicon ASIC bring-up. Hardware was for telecom network chipsets covering various standards including: T1/E1, DS3/E3, STS-1, SONET: OC-3, OC-12, OC-48. g.SHDSL, and VoIP.
- Set up a corporate wide Inventory, schematic, and footprint database for Mentor Graphic's Viewdraw/PADS system.

- Programmed miscellaneous code in C, Visual Basic, and Perl.
- Developed an Altera FPGA based SONET data capture PCI card capable of real-time capture of all traffic over the PCI bus.
- Developed a Bit Error Rate test card for fiber optic testing. Worked with our customer, Molex, to specify, design, and implement the PCB hardware and Altera FPGA controller.

Frasca International, Urbana, IL — Summer '98
https://www.frasca.com/
Electrical Engineering.

- Designed a PCI interface card to perform electronic control loading on flight simulators.
- Gained experience in selection and design using DACs, ADCs, and Resolver-to-Digital Converters.
- Selected PCB component, entered OrCad Schematic Capture, designed PCB layout, and practiced SMT hot air soldering.
- Programmed low-level code for real time operating systems in assembly and C.
- Debugged hardware BIOS conflicts with existing custom hardware and the Pentium II, providing a patch that allowed shipment of the flight simulator software with the latest generation PC hardware.

Beckman Institute, Theoretical Biophysics Group, Urbana, IL — Fall '97 – Spring '99
https://beckman.illinois.edu/
Programmer.

- Programmed numerical biophysical simulations in C++
- Worked on automated documentation of the numerical analysis of biophysical simulations.
- Gained experience using parallel processor SGI and HP machines. Including queuing and PVM operation.
- Learned and developed code in Java, CORBA, and Perl.

Innovative Legal Software, Arlington Heights, IL — Summer '97
Programmer.

- Developed custom form filling software for law firms.

Fermi National Accelerator Laboratory, Batavia, IL — Summer '96
https://www.fnal.gov/
Laboratory Assistant, Computing Division, Experimental Astrophysics Group.

- Worked with the Sloan Digital Sky Survey analyzing and calibrating photographic telescope data using digital CCD telescope data, in order to produce a uniform map of stars and galaxies suitable for statistical analysis.
- Wrote routines in Tcl and C to perform data reduction and analysis. Learned the workings of cross-platform standard data formats including FITS and TeX.
- Worked porting and cross-compiling C code between Silicon Graphics and DEC Alpha machines.

Fermi National Accelerator Laboratory, Batavia, IL — Summer '95
https://www.fnal.gov/
Laboratory Assistant, Computing Division, Experimental Astrophysics Group.

- Gained experience working in a large group environment. Responsibilities included C and Tcl programming and the use of the CVS software repository for version control.
- Installed, debugged, and created a user interface for a C based vector math package to replace the system of linked lists used by the Astrophysics Group on Silicon Graphics IRIX (Unix) hardware.
- Mastered HTML, CGI programming, Perl scripting, and Java/JavaScript.

AMCon Computers, Oak Park, IL — Summer '94
Hardware and Software Installation and Repair

- Installed Novell networks at small and medium sized businesses. Repaired computers.
- Debugged, on-site, the computers, networks, and software installations of individual and business clients.

Education

- *University of Illinois at Urbana-Champaign* https://illinois.edu/
  May 1999, Bachelor of Science in Computer Engineering.
  Program ranked second nationally by U.S. News & World Report (February 1998).
  Grade Point Average 3.7 of 4.0, James Scholar honors curriculum, Dean's List, six of eight semesters.
- *Northridge Prep*, Niles, Illinois. https://northridgeprep.org/
  May 1995, Graduated Salutatorian.
  Standardized scores: 1480 SAT (720V/760M), 31 ACT.

Relevant Computer Engineering Coursework

- **ECE 110** **Introduction to Electrical and Computer Engineering**
- **ECE 229** **Introduction to Electromagnetic Fields**. Covering Maxwell's equations, static fields, and waves.
- **ECE 249** **Digital Systems Laboratory**. Hands on exposure to digital logic design and implementation.

- **ECE 290** **Introduction to Computer Engineering**. Covering representation of information, combinatorial network analysis and design, sequential network analysis and design, computer organization and control, and machine-level programming.
- **ECE 291** **Computer Engineering, II**. Covering assembly language programming (80x86): I/O, interrupts, DMA, multitasking; low level graphics; real-time data acquisition and device control.
- **ECE 340** **Solid State Electronic Devices**. Covering P-N junctions; transistors; JFETs and MOS devices, etc.
- **ECE 312** **Computer Organization and Design**. Covering design, simulation, and layout of the control logic, arithmetic logic, and memory control logic of a pipelined MIPS processor using VHDL in Mentor Graphics.
- **ECE 310** **Digital Signal Processing.** Covering Z transform, FFT, DFT, stability, digital filter design.
- **ECE 311** **Microcomputer Laboratory.** Covering VHDL based design using Xilinx FPGAs , embedded processor design using the 80x86, video capture, ISA bus design, etc.
- **ECE 370** **Introduction to Robotics.** Homogeneous transformations etc. applied to robots in lab.
- **ECE 320** **Digital Signal Processing Laboratory.** Motorola 56302 based DSP implementations.
- **ECE 325** **Introduction to VLSI System Design.** CMOS logic design and chip layout in Mentor Graphics.
- **ECE 246** **Advanced Digital Projects Laboratory.** Open Lab. Working on real time USB audio processing.
- **ECE 342,3** **Electronic Circuits /w Laboratory.** Analog and digital circuit theory and design using BJTs, FETs, Op Amps, PSPICE, etc.

Released Shure Products with Major Contributions

- Axient Digital https://www.shure.com/en-US/products/wireless-systems/axient_digital
- Axient Digital Portable Receiver https://www.shure.com/en-US/products/wireless-systems/axient_digital/adx5d
- Axient Digital Micro Bodypack Transmitter https://www.shure.com/en-US/products/wireless-systems/axient_digital/adx1m
- ULX-D https://www.shure.com/en-US/products/wireless-systems/ulx-d_digital_wireless
- QLX-D https://www.shure.com/en-US/products/wireless-systems/qlx-d_digital_wireless
- SLXD https://www.shure.com/en-US/products/wireless-systems/slx_d_digital_wireless
- GLX-D+ https://www.shure.com/en-US/products/wireless-systems/glx-d_plus
- SUU https://www.shure.com/en-US/products/software/shure_update_utility
- Legacy: GLXD, Axient Analog, PGX

Additional Skills/buzzwords Related to Job Objective

- Established FPGA expertise in all major languages, vendors and tools: Altera, Xilinx, Lattice, Quartus, Vivado, Vitis HLS, Diamond, etc.
- Maintains a private hardware development lab at my residence to support remote work for Shure Incorporated, including hot-air solder equipment, binocular microscope, fume extraction, and full RF, analog, and digital lab bench.
- Experienced hardware PCB designer, capable of every step of the PCB flow including Schematic Entry, PCB design, 3D Mechanical Enclosure Design, SMD assembly, EMI design, High-speed digital design, analog design, RF design, FPGA design including logic design, timing analysis and closure, CDC design, modeling, simulation and bench-level board bring-up, system level debug, component level debug, and FPGA/ASIC bring up.
- Experienced 3D CAD designer (FreeCAD, Fusion 360) and manual metal worker with on site milling machine and proficiency with 3D Printing and CNC machining.
- Software, Embedded firmware and Android mobile expertise in C, C++, assembly, Python, Java, Javascript, Kotlin, go, Basic, and custom machine-code. Comfortable with architecting, designing and implementing all aspects of full applications including networking, graphics, database, etc..
- Experience with Linux, Ubuntu, Fedora, RHEL, Unix, DOS, ETS, VxWorks, and Windows, Git, bitbucket, subversion. Apache. VSCode. Gnu C++, Perl, Tcl, emacs, bash, gdb, whatever.
- Runs a home music composition and recording project studio.
- Plays Ice Hockey since 2020. Currently playing on the Polar Beers with HNA at the Edge Ice Arena in Bensenville.
- Raspberry PI. (Ask me about my Microsoft Teams meeting warning lights :-).